REMARKS

Claims 1-13 were pending. Responsive to the second Office Action, Claim 12 has been amended and Claim 13 canceled. Claims 1-12 are thus presented for further consideration.

Prosecution History

The application was filed with Claims 1-12. In the first Office action dated 12/10/01, Claims 1-12 were rejected. In a responsive amendment filed 3/12/02, Claim 11 was amended and Claim 13 was added.

In the second, non-final Office Action mailed on 1/2/03, Claims 1-13 were rejected. More particularly, Claims 1-5 and 7-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kizilyalli et al., "Deuterium Post-Metal Annealing of MOSFET's for Improved Hot Carrier Reliability," IEEE Electron Device Letters, Volume 18, No. 3, pp. 81-83 (March 1997), (hereinafter referred to as "*Kizilyalli*"), in view of U.S. Patent No. 6,328,801 issued to Gary et al. (hereinafter referred to as "*Gary*"). Additionally, Claim 6 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Kizilyalli* in view of *Gary* and U.S. Patent No. 6,159,829 issued to Warren et al. (hereinafter referred to as "*Warren*").

In response, Claim 12 has been amended and Claim 13 has been canceled. Claims 1-11 remain unchanged. The applicants respectfully traverse the foregoing rejections for the reasons hereinafter set out.

Requirements for *Prima Facie* Obviousness

The burden is on the Commissioner of Patents and Trademarks, acting through examining officials, to establish that an applicant is not entitled to a patent. The obligation of the examiner to go forward and produce reasoning and evidence in support of obviousness is clearly defined at M.P.E.P. §2142:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

A general definition of *prima facie* unpatentability is provided at 37 C.F.R. §1.56(b)(2)(ii):

> A *prima facie* case of unpatentability is established when the information *compels a conclusion* that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction

consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability. (emphasis added)

M.P.E.P. §2143 sets out the three basic criteria that the Examiner must meet to establish a *prima facie* case of obviousness:

1. some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;
2. a reasonable expectation of success; and
3. the teaching or suggestion of all the claim limitations by the prior art reference (or references when combined).

In the absence of such a *prima facie* showing of obviousness by the Examiner (assuming there are no objections or other grounds for rejection), an applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ 2d 1443, 1444 (Fed. Cir. 1992).

Thus, in order to support a *prima facie* obviousness rejection, the Examiner is obliged to produce evidence compelling a conclusion that each of the aforementioned three basic criteria has been satisfied.

Claims 1, 7, 11, 12 and 13

Kizilyalli is directed to hot carrier degradation in NMOS transistors. More particularly, applied voltage modulates the flow of carriers, *i. e.*, electrons, from one side of the transistor to another. The carriers splash over into the gate area because they are hot, and their presence degrades the interface between the gate dielectric and the silicon substrate. This degradation impairs the conductivity characteristics of the transistor, and causes it to operate outside of its performance specifications. The teaching of *Kizilyalli* is that "the hot carrier reliability (lifetime) of NMOS transistors annealed in deuterium can be increased by an order of magnitude over those annealed in hydrogen." (page 83, first sentence of the Conclusion)

Gary discloses a method and system for recovering and recirculating a deuterium-containing gas. Its teachings are used in conjunction with the annealing process during the manufacture of semiconductor devices, and particularly where a deuterium-containing annealing gas is used. "The pressure in process chamber 1 is controlled to a desired value by throttle valve 4 and pump 5." (col. 6, lines 27-28) Reference is made to "processes below atmospheric pressure, of from about 0.1 to 5 atmospheres." (col. 3, lines 43-44) The high cost and limited

availability of the deuterium isotope is noted in col. 2, lines 6-7. "The inventive method and system make the use of deuterium commercially feasible, and result in marked improvements in device lifetime as compared to hydrogen treatment." (Summary of the invention, last sentence)

As stated therein, Claims 1, 7, 11, and 12 are directed to radiation hardening a silicon-based semiconductor microcircuit. Neither *Kizilyalli* nor *Gary* teaches the problem posed by radiation to a silicon-based semiconductor microcircuit, or how to radiation harden such a microcircuit.

As stated in MPEP §2143.01:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPOQ2d 1430 (Fed. Cir. 1990).

As radiation hardening is not mentioned by either reference, there would have been no motivation for one of ordinary skill in the art to radiation harden a semiconductor microcircuit by annealing it in deuterium, as taught by *Kizilyalli*, in combination with "processes below atmospheric pressure" referenced in conjunction with the gas recirculation system and method of *Gary*. In the absence of such a reason or suggestion, their combination is improper and a *prima facie* case of obviousness cannot be made.

Claim 12 has been amended to more clearly avoid the cited references. Claim 13 has been canceled.

Claims 2, 3, 4, 5, 8, 9 and 10

The foregoing claims were rejected on the premise that, in view of *Kizilyalli* and *Gary*, "it would have been obvious to determine the optimum thickness, temperature as well as condition of the delivery of the layers involved." The aforementioned depending claims respectively recite values for temperature, time, and vacuum pressure, with the exception of Claim 5, which recites MOSFET devices. Although this rejection also lists independent Claim 11, the applicants believe this claim was mistakenly included herein because it was also included along with the other independent claims in the rejection of that group of claims.

The applicants acknowledge that discovery of the optimum value of a variable in a known process is normally obvious. *In re Antonie*, 559 F.2d 618, 620, 195 USPQ 6, 9 (CCPA1977). However, there is an exception to the foregoing rule when the optimized parameter is not recognized to be a result-effective variable. 559 F.2d at 620, 195 USPQ at 9. See *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955 (Fed. Cir. 1993). (Although an optimal condition would be met by fulfilling the claimed relationship, it was not inherent in the

prior art reference, nor were means to achieve this optimal condition disclosed, either explicitly or implicitly, by the reference. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient [to establish inherency]." (citation omitted))

As previously noted, *Kizilyalli* teaches increasing the hot carrier reliability (lifetime) of NMOS transistors, while *Gary* discloses a method and system for recovering and recirculating a deuterium-containing gas. Neither reference discusses or solves the problem of radiation. It follows that neither *Kizilyalli* nor *Gary*, either alone or in combination, show or suggest that the claimed values for temperature, time, and vacuum pressure, are result-effective variables for obtaining a radiation hardened semiconductor microcircuit. Thus, the applicants contend that the values set out in the foregoing claims present subject matter that is patentable over the cited references.

Claim 5 recites that the microcircuit includes MOSFET devices. The applicants respectfully submit that the Examiner's rejection based on the obviousness of optimum parameters is inappropriate because the claim does not recite parameters.

Claim 6

For the reasons previously set out in controverting the rejection of Claims 1, 7, 11, and 12, the applicants contend that it is improper to combine *Kizilyalli* and *Gary*. It follows that the rejection of Claim 6, as it relies on their being combined, is likewise improper.

Furthermore, *Warren* discloses processes intended to ensure the availability of mobile hydrogenous ions in a semiconductor further to transforming an ordinary semiconductor into an electronic memory device. More particularly, in Column 4, lines 34-37, *Warren* states that a charge in buried oxide layer 10 will cause the I-V curve to shift along the voltage axis, and that this voltage shift or hysteresis voltage is proportional to the charge density and depends on its spatial distribution in oxide layer 10. In column 4, lines 52-55, it further notes that the observed hysteretic behavior results from an electric field induced migration of a charged ionic species from one Si/SiO_2 interface to the other, and further suggests in column 4, line 67, that the mobile charge is H^+. *Warren* proceeds to teach that rapid cooling of the device from the anneal temperature enhances the introduction of the hydrogenous ions into oxide layer 10 that is necessary to obtain the desired hysteresis voltage.

The presence of positively charged ions, *e. g.*, hydrogenous ions, in a standard semiconductor microcircuit is undesirable because, among several deleterious effects, the ions

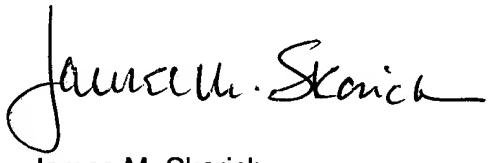
may move freely throughout the circuit and unpredictably change its performance and operating characteristics. Ensuring their availability teaches away from *Kizilyalli,* which discloses reducing the availability of hydrogen ions by annealing the semiconductor microcircuit in deuterium instead of hydrogen. The proposed modification is thus not proper, and *Warren* cannot be combined with *Kizilyalli* to support a *prima facie* obviousness rejection.

Conclusion

In view of the foregoing remarks, the applicants submit that Claims 1-12 presently in the application are patentably distinct over the cited references and in allowable form. Accordingly, the applicants earnestly solicit their favorable consideration and respectfully request that the application be passed to issue in its present condition.

Should the Examiner find any remaining impediment to the prompt allowance of the aforementioned claims that might be resolved or overcome with the aid a telephone conference, he is cordially invited to call the undersigned at the telephone number set out below.

Respectfully submitted,



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R duction of hot el ctron d gradation in m tal oxid semiconductor transistors by d uterium proc ssing

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We report experimental results that replacing hydrogen with deuterium during the final wafer sintering process greatly reduces hot electron degradation effects in metal oxide semiconductor transistors due to a new giant isotope effect. Transistor lifetime improvements by factors of 10–50 are observed. A plausible physical theory suggests that the benefits of deuterium use may be general and also applicable to other areas of semiconductor device processing and fabrication. © *1996 American Institute of Physics.* [S0003-6951(96)00418-4]

The time-dependent degradation of metal oxide semiconductor (MOS) transistor performance resulting from hot (energetic) electron effects has been an area of considerable study over the past 25 years.[1] According to established theory, this aging process is thought to occur in part as the result of hot electrons stimulating the desorption of hydrogen from the Si/SiO_2 interface region. Hydrogen is introduced by necessity during several device processing steps as, for example, during the sintering of the wafers at elevated temperature in a hydrogen ambient.[2] While this process improves device function, it sets the stage for subsequent hot electron degradation. In this letter we demonstrate an alternative process in which the interface states are passivated by deuterium instead of hydrogen. Transistors that have been annealed with deuterium show a greatly reduced degradation due to hot electron effects.

The idea of using deuterium instead of hydrogen was in part inspired by experiments in which a scanning tunneling microscope (STM) was used to stimulate the desorption of hydrogen from Si(100)2×1:H surfaces under ultrahigh vacuum (UHV) conditions.[3] Following the suggestion of Avouris,[4] these experiments were extended to deuterated surfaces in order to explore more fully the surface science issues of this process. From these new experiments it was discovered that deuterium is much more difficult to remove under the conditions used to desorb hydrogen.[5] While there are clearly many differences between a free surface in UHV and a buried Si/SiO_2 interface, this result suggests the possibility for a sizable isotope effect if hydrogen is replaced by deuterium during the conventional wafer sintering step. To test for the advantages of using deuterium, uncapped complementary metal oxide semiconductor (CMOS) wafers fabricated at Bell Laboratories were subjected to the deuterium sintering process at Illinois and then returned to Bell Laboratories for electrical stress testing.

The wafers used for our tests contained *n*-channel metal oxide semiconductor (NMOS) transistor structures fabricated using the Bell Laboratories 0.5 μm 3.3 V CMOS technology.[6] However, the following three changes were made: (i) the gate oxide was reduced to $t_{ox} \sim 55$ Å, (ii) the doping in the *p*-well was increased, and (iii) the phosphorus doped lightly doped drain region was replaced by a shallow arsenic implanted (dose = 4×10^{14} cm^{-2} and energy = 30 keV) source-drain extension region. These process modifications enhance the peak value for the source-drain electric field near the drain edge of the gate, resulting in more channel hot electrons. The shallow source-drain extension ensures that these hot electrons are near the Si/SiO_2 interface, where they will cause significant interface damage. The interface damage, caused by these hot carriers, can easily be observed by monitoring the change in the NMOS transistor transconductance (i.e., $g_m = \Delta I_{DS}/\Delta V_{GS}|_{V_{DS}=0.1\ \mathrm{V}}$) or by the shift in the transistor threshold voltage V_{TH}.[7]

For this study, accelerated hot carrier dc stress experiments were performed on transistors with varying gate lengths (0.5–15 μm) at peak substrate current conditions. The applied (accelerated) stress source drain voltage was $V_{DS}=5$ V and the source gate voltage was $V_{GS}=2$ V. Stress experiments performed at lower voltages ($V_{DS}=3.8$ V and $V_{GS}=1.5$ V) and shorter gate lengths (0.3 and 0.4 μm) give results similar to the ones reported below. Prestress transistor measurements demonstrate that devices sintered in hydrogen or deuterium have identical electrical characteristics (e.g., transconductance, subthreshold slope, threshold voltage, saturation current, substrate current, etc.).

Figure 1 shows the g_m degradation as a function of stress time for NMOS transistors with five gate lengths ranging from 0.5 to 0.7 μm. Figure 2 shows the threshold voltage increase as a function of stress time for the same devices. All of these transistors are from the same wafer and were processed identically except for the manner in which they were sintered. Wafers sintered in deuterium exhibit much more resilience to channel hot carrier stress. In our comparative study, we have electrically stressed 80 or so transistors, and have observed the same strong trend. These results have also been verified by performing the same electrical stress experiments on a second wafer from another lot. If we use 20% g_m degradation as a lifetime criterion, transistors sintered in deuterium typically have lifetimes 10–50 times longer than those sintered in hydrogen. Likewise, we observe a factor of 10 improvement in lifetime if we take a shift of 200 mV in threshold voltage as the degradation criterion. In our opinion,

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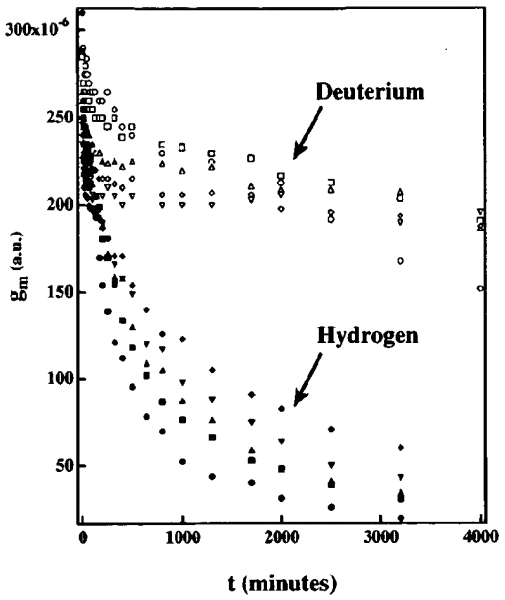

FIG. 1. Comparative time-dependent degradation of the transconductance g_m for five NMOS transistors sintered in hydrogen (solid symbols) and deuterium (unshaded symbols). The sinter process was performed in a 90% N_2:10% $H_2(D_2)$ ambient at 400 °C for 1 h.

further improvements in lifetime will be achieved once the optimum sinter process conditions are determined.

The theoretical explanation of the reduced hot electron degradation due to deuterium treatment is probably analogous to the explanation for the STM experiments by Avouris *et al.*,[8] although this analogy should not be pushed too far. They showed that hydrogen absorbed on the silicon surface can be taken off by a STM tip up to 100 times easier than deuterium. An explanation of such a giant isotope effect can be found by assuming that the hot electrons cause a population of a silicon hydrogen (deuterium) antibonding state. This results in a force that accelerates the hydrogen away from the silicon surface leading to reduced wave function overlap with bulk silicon states. That acceleration is, of course, much diminished for the deuterium because of its bigger mass. For the same reason the kinetic energy gain necessary for dissociation is reached faster by hydrogen than by deuterium. In other words, the differences between hydrogen and deuterium arise from dynamic effects as they are important in chemical reactions. The static chemical bonding is evidently the same for both hydrogen and deuterium which is the reason for the identical transistor properties after hydrogen and deuterium treatment before hot electron dynamics and resultant damage. The difference of the hot electron degradation compared to the STM experiment lies mainly in the more complex chemistry of the Si/SiO_2 interface. The hydrogen (deuterium) passivating a silicon bond may (due to hot electron excitation) transfer to the SiO_2, passivating a more removed silicon bond or linking up with oxygen or even forming H_2 (D_2). All of these processes may be complicated by processes of interface reconstruction and defect chemistry. As a consequence, the energy needed to depassivate and remove hydrogen (deuterium) may be significantly different from the energies in the STM experiments. The close proximity of SiO_2 (instead of the more remote tip) will also permit different reactions of hydrogen (deuterium) than the "reaction" with the tip electrode.

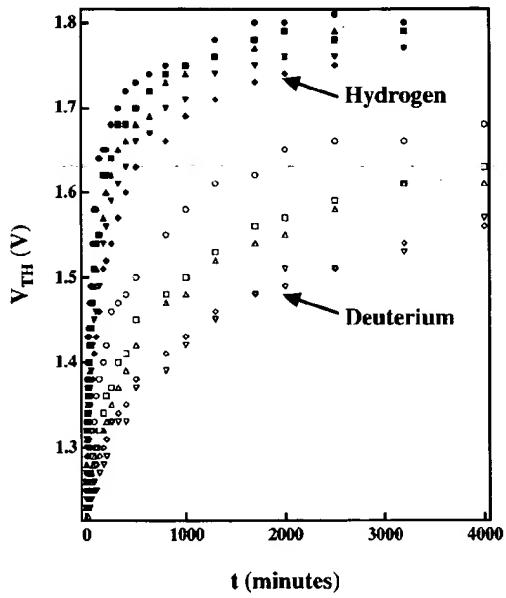

FIG. 2. Comparative time-dependent increase of the threshold voltage V_{th} for NMOS transistors sintered in hydrogen (solid symbols) and deuterium (unshaded symbols). These are the same five devices shown in Fig. 1.

In addition to the effects discussed above there are also other effects that may explain the large improvement of hot electron degradation by use of deuterium. One effect is the well-known isotope effect that relates to the larger zero point energy of the Si–H oscillations as compared to Si–D. Another effect is the possibility of excited Si–H or Si–D oscillations. Hot electrons in devices may excite by multiple impact oscillations far above the thermal equilibrium and thus force dissociation. A multiple excitation mechanism is also thought to explain hydrogen desorption at lower electron energies in the STM experiments.[9] Again, deuterium would show less energy transfer because of its large mass. Another explanation is related to the possible mass dependence of tunneling of the nuclei that might be involved in the chemical process of dissociation. We do not want to speculate at this point on which effect is dominant. All of these effects favor deuterium as the more stable passivation. The generality of these effects suggests that deuterium instead of hydrogen may be beneficial in other processes, devices, and device materials. Note that the well-known effects based on differing mobilities of H^+ and D^+ (e.g., following gamma irradiation[10]) or as occurring in electrolysis will not explain the giant isotope effect that we observe. These effects do not involve hot electrons at the interface.

In conclusion, we have demonstrated that the replacement of hydrogen with deuterium during the final wafer sintering process results in substantially reduced susceptibility to hot electron degradation effects. The explanation of the effect is based on the increased difficulty to break the deuterium bond due to the additional neutron mass.

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